LISTING OF CLAIMS

1. (Currently Amended) A **processor-implemented** method comprising:

receiving a ~~first~~ **binary** sequence of values**, the values to be used in an application as a varying-radix sequence of values, the varying-radix sequence of values to represent bit distribution information for the binary sequence of values**;

~~determining a number of positions for a second sequence of values;~~ and

generating the ~~second~~ **varying-radix sequence of values from the binary sequence of values via a radix unit executed by the processor, the radix unit to**

determine a number of positions for the varying-radix sequence of values,

determine the maximum radix for the varying-radix sequence of values, **the maximum radix based on a set of rules for the application,**

determine the remaining radices for the varying-radix sequence of values based on the maximum radix and the set of rules for the application, and

determine a ~~each~~ value **for each position** of the ~~second~~ **varying-radix** sequence **of values** ~~corresponding to a radix, the radix for each value of the second sequence varying over the second sequence in relation to an application value, the application value corresponding to a position in the second sequence and a sum of a set of values in the second sequence~~.

2-5. (Cancelled).

6. (Currently Amended) The method of claim 1 further comprising:

converting the ~~second~~ **varying-radix** sequence **of values** into a decimal value;

converting the decimal value into a**n additional** binary sequence;

transmitting the **additional** binary sequence and the number of positions;

restoring the **additional** binary sequence to the decimal value;

generating the ~~second~~ **varying-radix** sequence **of values** from the decimal value **and the number of positions**; and

reconstructing the ~~first~~ **binary** sequence from the ~~second~~ **varying-radix** sequence **of values**.

7-16. (Cancelled).

17. (Currently Amended) A machine-readable **storage** medium that provides instructions, which when executed by a set of one or more processors, cause said set of processors to perform operations comprising:

receiving a ~~first~~ **binary** sequence of values**, the values to be used in an application as a varying-radix sequence of values, the varying-radix sequence of values to represent bit distribution information for the binary sequence of values**;

~~determining a number of positions for a second sequence of values;~~ and

generating the ~~second~~ **varying-radix sequence of values from the binary sequence of values via a radix unit executed by the processor, the radix unit to**

determine a number of positions for the varying-radix sequence of values,

determine the maximum radix for the varying-radix sequence of values, **the maximum radix based on a set of rules for the application,**

determine the remaining radices for the varying-radix sequence of values based on the maximum radix and the set of rules for the application, and

determine each value **for each position** of the ~~second~~ **varying-radix** sequence **of values** ~~corresponding to a radix, the radix for each value of the second sequence varying over the second sequence in relation to an application value, the application value corresponding to a position in the second sequence and a sum of a set of values in the second sequence~~.

18-21. (Cancelled).

22. (Currently Amended) The machine-readable **storage** medium of claim 17 further comprising:

converting the ~~second~~ **varying-radix** sequence **of values** into a decimal value;

converting the decimal value into a**n additional** binary sequence;

transmitting the **additional** binary sequence and the number of positions;

restoring the **additional** binary sequence to the decimal value;

generating the ~~second~~ **varying-radix** sequence **of values** from the decimal value **and the number of positions**; and

reconstructing the ~~first~~ **binary** sequence from the ~~second~~ **varying-radix** sequence **of values**.

23-25. (Cancelled).

26. (New) An apparatus comprising:

a processor to receiving a binary sequence of values, the values to be used in an application as a varying-radix sequence of values, the varying-radix sequence of values to represent bit distribution information for the binary sequence of values; and

a radix unit operatively coupled to the processor to generating the varying-radix of values from the binary sequence of values via a radix unit executed by the processor, wherein generating the varying-radix sequence of values includes

determining a number of positions for the varying-radix sequence of values,

determining the maximum radix for the varying-radix sequence of values, the maximum radix based on a set of rules for the application,

determining the remaining radices for the varying-radix sequence of values based on the maximum radix and the set of rules for the application, and

determining each value for each position of the varying-radix sequence of values.

27. (New) The apparatus of claim 26, the processor to further

convert the varying-radix sequence of values into a decimal value,

convert the decimal value into an additional binary sequence,

transmit the additional binary sequence and the number of positions,

restore the additional binary sequence to the decimal value,

generate the varying-radix sequence of values from the decimal value and the number of positions, and

reconstructing the binary sequence from the varying-radix sequence of values.

28. (New) The apparatus of claim 26, wherein the application includes a First In Last Out (FILO) stack and the binary sequence represents a sequence of operations on the FILO stack.

29. (New) The apparatus of claim 26, wherein the application includes a Multi-Pulse Excited Linear Prediction (MPELP) speed codec.

30. (New) The method of claim 1, wherein the application includes a First In Last Out (FILO) stack and the binary sequence represents a sequence of operations on the FILO stack.

31. (New) The method of claim 1, wherein the application includes a Multi-Pulse Excited Linear Prediction (MPELP) speed codec.

32. (New) The machine-readable storage medium of claim 17, wherein the application includes a First In Last Out (FILO) stack and the binary sequence represents a sequence of operations on the FILO stack.

33. (New) The machine-readable storage medium of claim 17, wherein the application includes a Multi-Pulse Excited Linear Prediction (MPELP) speed codec.